IN THE CLAIMS

Claims 1-7 are cancelled.

8. (Currently Amended) ~~A~~ The method according to Claim ~~7~~19, wherein:

for those circuits that fail both the further timing analysis and the further soft error analysis, the step of further improving the circuits includes the step of increasing the voltage applied to the circuits; and

for those circuits that pass the further timing analysis and fail the further soft error analysis, the step of further improving the circuits includes the step of increasing the capacitance of the circuits.

Claims 9-18 are cancelled.

Please add the following new claims:

19. (New) A method of simulating an integrated circuit, the method comprising the steps of:

performing a timing analysis of the circuits to ensure that they meet specified timing criteria;

performing soft error analysis of the circuits to determine whether they meet specified soft error criteria;

improving those circuits that fail the soft error analysis to improve their resistance to soft errors;

performing a further timing analysis of the improved circuits to determine whether the improved circuits still meet the specified timing criteria;

performing a further soft error analysis of the improved circuits to determine whether the improved circuits now meet the soft error criteria; and

further improving those circuits that fail the further soft error analysis using one of two defined procedures depending on whether the circuits pass or fail the further timing analysis.

20. (New) A method of simulating an integrated circuit, the method comprising the steps of:

performing soft error analysis of the circuits to determine whether they meet specified soft error criteria;

improving those circuits that fail the soft error analysis to improve their resistance to soft errors;

performing a further soft error analysis of the improved circuits to determine whether the improved circuits now meet the soft error criteria; and

further improving those circuits that fail the further soft error analysis using one of at least two defined procedures depending on whether the circuits pass or fail the further timing analysis.

21. (New) A system for simulating an integrated circuit, the system comprising:

means for performing a timing analysis of the circuits to ensure that they meet specified timing criteria;

means for performing soft error analysis of the circuits to determine whether they meet specified soft error criteria;

means for improving those circuits that fail the soft error analysis to improve their resistance to soft errors;

means for performing a further timing analysis of the improved circuits to determine whether the improved circuits still meet the specified timing criteria;

means for performing a further soft error analysis of the improved circuits to determine whether the improved circuits now meet the soft error criteria; and

means for further improving those circuits that fail the further soft error analysis using one of two defined procedures depending on whether the circuits pass or fail the further timing analysis.

22. (New) A system for simulating an integrated circuit, the method comprising the steps of:

means for performing soft error analysis of the circuits to determine whether they meet specified soft error criteria;

means for improving those circuits that fail the soft error analysis to improve their resistance to soft errors;

means for performing a further soft error analysis of the improved circuits to determine whether the improved circuits now meet the soft error criteria; and

means for further improving those circuits that fail the further soft error analysis using one of at least two defined procedures depending on whether the circuits pass or fail the further timing analysis.

23. (New) A program storage device readable by a machine, tangibly embodying a program of instructions executable by the machine to perform method steps for simulating an integrated circuit, the method steps comprising:

performing a timing analysis of the circuits to ensure that they meet specified timing criteria;

performing soft error analysis of the circuits to determine whether they meet specified soft error criteria;

improving those circuits that fail the soft error analysis to improve their resistance to soft errors;

performing a further timing analysis of the improved circuits to determine whether the improved circuits still meet the specified timing criteria;

performing a further soft error analysis of the improved circuits to determine whether the improved circuits now meet the soft error criteria; and

further improving those circuits that fail the further soft error analysis using one of two defined procedures depending on whether the circuits pass or fail the further timing analysis.

24. (New) A program storage device readable by a machine, tangibly embodying a program of instructions executable by the machine to perform method steps for simulating an integrated circuit, the method steps comprising:

performing soft error analysis of the circuits to determine whether they meet specified soft error criteria;

improving those circuits that fail the soft error analysis to improve their resistance to soft errors;

performing a further soft error analysis of the improved circuits to determine whether the improved circuits now meet the soft error criteria; and

further improving those circuits that fail the further soft error analysis using one of at least two defined procedures depending on whether the circuits pass or fail the further timing analysis.

DRAWING OBJECTIONS

Drawings 1-3 were objected to for not including the legend Prior Art. These drawings have been amended to include this legend as indicated in the attached Drawing Change Authorization Request. No new matter is being added.

CLAIM OBJECTIONS

Claims 1-18 were objected for the various reasons stated in the current Office Action. Claims 1-7 and 9-18 have been cancelled. Claim 8 has been amended as suggested by the Examiner.

CLAIM REJECTIONS

Claims 1-6 and 10-18 were rejected under 35 U.S.C Sections 102 and 103 as stated in the current Office Action. Claims 1-6 and 10-18 have been cancelled.